CLAIMS

What is Claimed Is:

1. A process for forming a resistance structure comprising the steps of:

a) depositing a first layer of aluminum;

b) oxidizing the surface of said first layer of aluminum defining an oxidized layer; and

c) depositing a second layer of aluminum on said oxidized layer forming a resistance structure.

2. The process as recited in claim 1, wherein said resistance structure is formed as a vertical resistance structure.

3. The process as recited in claim 1, wherein said resistance structure is formed as a planar structure.

4. The process as recited in claim 1, wherein said resistance structure is formed in a step configuration.

5. The process as recited in claim 1, wherein said oxidizing step includes controlling the oxygen pressure during oxidation.

6. The process as recited in claim 5, wherein said oxidation pressure is controlled in order to control the resistance of said resistance structure.

7. The process as recited in claim 1, further including the step of cleaning said second layer of aluminum.

8. The process as recited in claim 7, wherein said cleaning step includes ion beam etching.

9. The process as recited in claim 7, wherein said cleaning step includes RF plasma etching.

10. The process as recited in claim 1, further including the step of doping said second layer of aluminum.

11. The process as recited in claim 10, wherein said doping step includes doping said second layer of aluminum with paramagnetic impurities.

12. The process as recited in claim 10, wherein said doping step includes doping said second layer of aluminum with oxygen.

13. The process as recited in claim 10, wherein said doping step includes doping said second layer of aluminum with nitrogen.

14. A process for forming a resistance structure comprising the steps of:

a) depositing a first layer of aluminum;

b) oxidizing the surface of said first layer of aluminum defining an oxidized layer; and

c) depositing a material on said oxidized layer to prevent superconducting tunneling.

15. The process as recited in claim 14, wherein step c includes depositing titanium on said oxidized layer.

16. The process as recited in claim 14, wherein step c includes depositing molybdenum on said oxidized layer.

17. The process as recited in claim 14, wherein step c includes depositing nitrogen on said oxidized layer.

18. The process as recited in claim 14, wherein step c includes depositing niobium nitride on said oxidized layer.

19. A resistance structure adapted to be formed on an integrated circuit, the resistance structure comprising:

a first layer of aluminum;

a layer of aluminum oxide;

a second layer of aluminum, configured such that said layer of aluminum oxide is sandwiched between said first and second layers of aluminum.

20. The structure as recited in claim 13, wherein said second layer of aluminum is doped.

21. The structure as recited in claim 20, wherein said second layer of aluminum is doped with oxygen.

22. The structure as recited in claim 20, wherein said second aluminum layer is doped with nitrogen.

23. A resistance structure adapted to be formed on an integrated circuit, the resistance structure comprising:

a first layer of aluminum;

a layer of aluminum oxide defining an oxide layer; and

a layer formed on top of said oxidized layer, formed from a material selected to prevent superconducting tunneling.

24. The resistance structure as recited in claim 23, wherein said material is at least 30 nm of aluminum.

25. The resistance structure as recited in claim 23, wherein said material is aluminum doped with paramagnetic impurities.

26. The resistance structure as recited in claim 23, wherein said material is aluminum doped with oxygen.

27. The resistance structure as recited in claim 23, wherein said material is aluminum doped with nitrogen.

28. The resistance structure as recited in claim 23, wherein said material is titanium.

29. The resistance structure as recited in claim 23, wherein said material is molybdenum.

30. The resistance structure as recited in claim 23, wherein said material is niobium nitride.

31. A process for forming a resistance structure, the process comprising the steps of:

(a) providing a substrate;

(b) depositing a first niobium layer on said substrate;

(c) depositing a first aluminum layer on said niobium layer;

(d) allowing a portion of said aluminum layer to oxidize forming an oxidized layer;

(e) depositing a second aluminum layer on said oxidized layer;

(f) depositing a second niobium layer on said second aluminum layer forming a pentalayer structure;

(g) etching said pentalayer structure to remove said second niobium layer;

(h) depositing a third niobium layer on said second aluminum layer forming an aluminum/niobium bilayer;

(i) depositing and developing a photoresist on said bilayer to define a top portion of a vertical resistor;

(j) etching said third layer of niobium to expose said second aluminum layer defining an exposed aluminum layer;

(k) applying a dielectric on top of said second niobium layer and said exposed aluminum layer;

(l) etching said dielectric to form a via to said second aluminum layer; and

(m) depositing a niobium interconnect layer.

32. A process for forming a resistance structure comprising the steps of:

a) providing a substrate;

b) depositing a first niobium layer on a portion of said substrate;

c) depositing a first aluminum layer on said first niobium layer;

d) allowing a portion of said first aluminum layer to oxidize forming an oxidized layer;

e) depositing a second aluminum layer on said oxidized layer;

f) depositing a dielectric on a portion of said second aluminum layer and said substrate defining an exposed portion of said second aluminum layer; and

g) depositing a second niobium layer on top of said exposed portion of said second aluminum layer and said dielectric.

33. A process for forming a resistance structure comprising the steps of:

(a) providing a substrate;

(b) depositing a layer of NbN on a portion of said substrate;

(c) depositing a dielectric on said NbN layer;

(d) depositing a first layer of aluminum on said dielectric layer and on said substrate adjacent said NbN layer forming a step;

(e) allowing a portion of said first aluminum layer to oxidize defining an oxidized layer; and

(f) depositing a second layer of aluminum on said oxidized layer.